AMENDMENT TO CLAIMS

Please **ADD** new claims 27-40 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Previously Presented) A method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor and a p-type transistor on a semiconductor wafer, the method comprising:

covering the p-type transistor with a mask;

oxidizing a portion of the gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor; and

removing, after the oxidizing step, oxide formed during the oxidizing step from above the gate polysilicon of the n-type transistor,

wherein the oxidizing step results in formation of a bird's beak in an edge of the gate polysilicon between the gate polysilicon and a spacer of the n-type transistor and the removing step preserves the bird's beak.

2. (Original) The method of claim 1, wherein the step of covering comprises covering the p-type transistor with a mask made of nitride.

3. (Original) The method of claim 1, wherein the step of oxidation is performed using low temperature oxidation.

4. (Original) The method of claim 1, wherein the step of oxidation is performed using at least one of high pressure oxidation or atomic oxidation or plasma oxidation.

5. (Original) The method of claim 1, wherein the step of oxidation is performed between a temperature of about 25°C to about 600°C.

6. (Original) The method of claim 1, further comprising forming a planarized oxide layer on the semiconductor wafer.

7. (Original) The method of claim 6, further comprising removing silicide material from above the gate polysilicon of the n-type field effect transistor.

8. (Original) The method of claim 7, wherein the step of removing silicide material from above the gate polysilicon of the n-type field effect transistor comprises etching the silicide material from above the gate polysilicon of the n-type field effect transistor.

9. (Previously Presented) The method of claim 1, wherein the removing step comprises removing a deposited oxide from above the gate polysilicon of the n-type field effect transistor by etching the deposited oxide from above the gate polysilicon of the n-type field effect transistor.

10. (Previously Presented) A method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor and a p-type transistor on a semiconductor wafer, the method comprising:

covering the p-type transistor with a mask;

oxidizing a portion of a gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor, wherein the oxidizing results in formation of a bird's beak in an edge of the gate polysilicon;

removing, after the oxidizing step, oxide above the gate polysilicon of the n-type transistor, the removing step comprising removing a deposited oxide from above the gate polysilicon of the n-type field effect transistor by etching the deposited oxide from above the gate polysilicon of the n-type field effect transistor; and

depositing silicide material on at least the portion of the gate polysilicon of the n-type field effect transistor.

11. (Previously presented) The method of claim 10, wherein the step of depositing silicide forming material on at least the portion of the gate polysilicon of the n-type field effect transistor comprises depositing at least one of Co, Hf , Mo, Ni, Pd_2, Pt, Ta, Ti, W, and Zr.

12. (Original) The method of claim 10, further comprising removing the mask used to cover the p-type field effect transistor.

13. (Original) The method of claim 1, further comprising depositing at least one of a silicide material or a nitride cap on at least the gate polysilicon of the n-type field effect transistor and removing silicide material or the nitride cap from above the gate polysilicon of the n-type field effect transistor prior to performing the step of oxidizing.

14. (Original) The method of claim 1, wherein the step of oxidizing comprises oxidizing the gate polysilicon of the n-type field effect transistor to create a stress of about 700MPa in a channel of the n-type field effect transistor.

15. (Original) The method of claim 1, wherein the step of oxidizing comprises oxidizing the gate polysilicon of the n-type field effect transistor to create tensile mechanical stresses are about 500Pa to about 1000Pa.

16. (Previously Presented) A method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type field effect transistor and a p-type field effect transistor on a semiconductor wafer, the method comprising forming oxide between a side of a gate polysilicon and a spacer of the n-type field effect transistor, oxidizing a portion of a the gate polysilicon of the n-type field effect transistor, such that tensile mechanical stresses are formed within a channel of the n-type field effect transistor, without creating additional tensile stresses in a channel of the p-type field effect transistor, and removing oxide formed during the oxidizing step from above the gate polysilicon of the n-type field effect transistor, wherein the oxidizing step results

in formation of a bird's beak in an edge of the gate polysilicon between the gate polysilicon and the spacer and the removing step preserves the bird's beak.

Claims 17-20 (Cancelled).

21. (Previously Presented). The method of claim 1, wherein the step of oxidizing a portion of a gate polysilicon of the n-type transistor is performed after silicidation of the gate polysilicon.

22. (Previously Presented) The method of claim 1, wherein the tensile stresses are formed along a longitudinal direction of the channel of the n-type transistor.

Claim 23 (Canceled).

24. (Previously Presented) A method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor and a p-type transistor on a semiconductor wafer, the method comprising:

forming a first oxide above a gate polysilicon and between a side of the gate polysilicon and a spacer of the n-type transistor,

masking the p-type transistor;

removing the first oxide from above the gate polysilicon of the n-type transistor while allowing the first oxide to remain between the side of the gate polysilicon and the spacer,

oxidizing a portion of a the gate polysilicon of the n-type transistor, such that tensile mechanical stresses are formed within a channel of the n-type transistor; and

removing the oxide formed during the oxidizing from above the gate polysilicon of the n-type transistor,

wherein, after the removing of the oxide formed during the oxidizing, a bird's beak remains in the gate polysilicon between the gate polysilicon and the spacer of the n-type transistor.

25. (Previously Presented) The method of claim 24, wherein the oxidizing step forms the bird's beak and the removing step preserves the bird's beak.

26. (Previously Presented) The method of claim 1, further comprising forming oxide between a side of the gate polysilicon and the spacer of the n-type transistor.

27. (New) A method of forming a device, comprising:

forming a PFET and NFET structure each having polysilicon gate structures;

depositing a metal or a low resistance material to a thickness of about 30Å to about 200Å across the polysilicon gate structures and exposed surfaces;

removing unreacted metal while formed silicide remains on the polysilicon gate structures;

planarizing an oxide fill formed over the silicide;

removing the silicide on top of the polysilicon gate structures using a selective etch;

protecting the PFET polysilicon gate structures and exposing the NFET polysilicon gate structures;

oxidizing the NFET, while protecting the PFET with a mask, such that the polysilicon gate structures of the PFET are not oxidized while oxide is deposited on the polysilicon gate structures of the NFET resulting in a formation of a vertical bird's beak in an edge of polysilicon of the polysilicon gate structures of the NFET.

28. (New) The method of claim 27, wherein the silicide is formed from reacting an underlying layer with Co, Hf, Mo, Ni, Pd2, Pt, Ta, Ti, W, or Zr.

29. (New) The method of claim 27, wherein the forming of the silicide is a self-aligned silicide process.

30. (New) The method of claim 27, wherein the mask is a hard mask made of nitride.

31. (New) The method of claim 30, wherein the nitride covering the polysilicon gate structures of the NFET is etched to expose the polysilicon gate structures of the NFET.

32. (New) The method of claim 27, wherein the oxidation of the polysilicon gate structures of the NFET creates tensile stresses in a channel region of the NFET.

33. (New) The method of claim 27, wherein the tensile stresses increase electron mobility along the channel.

34. (New) The method of claim 27, wherein the oxidation of the polysilicon gate structures of the NFET is performed at a temperature of 600°C or less to prevent degradation of device characteristics.

35. (New) The method of claim 27, wherein the oxidation results in about a vertically formed bird's beak of about 20Å to about 100Å in width and height.

36. (New) The method of claim 27, wherein the vertical bird's beak causes a base of the polysilicon to be wider than an uppermost surface of the polysilicon and side edges of the polysilicon taper towards the uppermost surface.

37. (New) The method of claim 36, wherein deposited oxide forming the vertical bird's beak is present along a plane perpendicular to a plane of the base of the polysilicon.

38. (New) The method of claim 27, wherein the oxide above the polysilicon gate structures of the NFET is etched off while the vertical bird's beak is preserved.

39. (New) The method of claim 38, wherein stresses created in the polysilicon gate structure of the NFET are maintained after removal of the oxide on top of the polysilicon as a result of the vertical bird's beak formed in the gate polysilicon structures of the NFET.

40. (New) The method of claim 27, further comprising:
growing an oxide on the polysilicon gate structures;
forming spacers sidewalls of the polysilicon gate structures; and
forming source and drain regions for the polysilicon gate structures.